

Investigation into PCB Routing Loss for Coupled Inductor Based VR (Voltage Regulator) Design in Server Computing System

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Abstract

Coupled inductor is one appealing technology to improve transient response and reduce output decoupling significantly in interleaved multi-phase voltage regulators (VRs). One well known problem is that coupled inductor winding structure causes PCB routing path longer than discrete inductor design. This paper investigates possible PCB routing schemes for coupled inductor and conducts a fair and quantitative comparison with discrete inductor in a server VR design. Simulation and measurement are also conducted to verify the analysis.

Keywords

PCB Routing Loss, Coupled Inductor, Voltage Regulator (VR), Server

1. Introduction

According to the microprocessor's roadmap, there are several stringent challenges for the future microprocessor voltage regulators (VRs): high output current, low output voltage, high current slew rate and low droop resistance. These challenges require the VRs to have both higher steady state performance and faster transient performance. To improve above issues in today's multiphase non-coupled VRs, inversely coupled inductor VRs are proposed mainly to improve transient response significantly so that both real estate and cost could be saved on output decoupling [1] [2]. Some studies also shows that inversely coupled inductor could also help improve VR's conversion efficiency if keeping the same transient response as non-coupled multiphase VRs [3] [4]. With all these advantages, as shown in **Figure 1**, one well-known issue for coupled inductor based VR design is that inversely coupled structure of the inductor

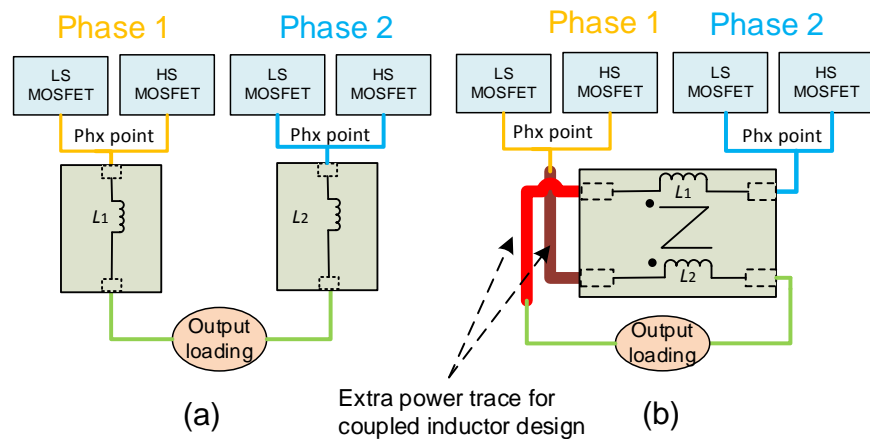


Figure 1. Layout trace difference for discrete inductor vs. coupled inductor design (a) discrete inductor; (b) coupled inductor.

winding will make overall length of PCB routing trace longer than discrete inductor design, thus causes higher PCB trace impedance to have side effect on VR efficiency. As shown in **Figure 1(b)**, the thick solid line illustrates extra power trace in a typical inversely coupled inductor design. It's a concern especially in such high current load application as server CPU core VRs. Previous papers have discussed some proposals to address this problem by adopting a new twisted magnetic core structure for coupled inductor [5] [6], however it's complicated from implementation viewpoint and not friendly for mass production to benefit industry. Moreover, there is still lacking of quantitative study of side impact on VR conversion efficiency from aforementioned problem by using coupled inductor. This paper has a detailed investigation into a real coupled inductor based server VR design, simulates the DC impedance of coupled inductor winding path with different layout schemes, compares the DC impedance of coupled inductor winding path with discrete inductor counterpart as well, finally conducts an quantitative analysis for the exact efficiency impact for coupled inductor design.

2. Layout Improvements for Coupled Inductor Design for a Server CPU VR

To meet both power integrity (PI) and signal integrity (SI) requirement, server real mother board is typically designed with 10 - 12 layers PCB stackup today and all internal layers are normally 1oz copper thickness while top and bottom layers are 1.5oz, and 10 layers motherboard design is more popular. One coupled inductor VR power evaluation board is built as a baseline for the analysis in this paper. It's built with 8 layers stackup to emulate real 10 layers situation in server motherboard. As shown in **Figure 2**, top and bottom layers are 1.5oz, internal layers are all 1oz except 2oz for layer 4 and layer 5. This stackup is equivalent to server 10 layers design (usually with two more 1oz GND layers) so that the analysis could be representative of real server motherboard application.

Layer Name	Plane Description	Layer Thickness (mil)	Copper Weight (oz)	Dielectric (eR)
	solder mask	0.5		3.8
Signal 1(L1)	SIGNAL	1.9	1.5	
	prepreg	2.7		4.0
Plane 2(L2)	GND	1.3	1.0	
	core	4		4.1
Signal 3(L3)	Sig/pwr	1.3	1.0	
	prepreg	15		4.0
Plane 4(L4)	Pwr/gnd	2.6	2.0	
	core	4		4.1
Plane 5(L5)	Gnd	2.6	2.0	
	prepreg	15		4.0
Signal 6(L6)	Sig/gnd	1.3	1.0	
	core	4		4.1
Plane 7(L7)	GND	1.3	1.0	
	prepreg	2.7		4.0
Signal 8(L8)	SIGNAL	1.9	1.5	
	solder mask	0.5		3.8
	total	62.6	+8/-5	

Figure 2. Layout trace difference for discrete inductor vs. coupled inductor design (a) discrete inductor; (b) coupled inductor.

In server form factor design, the height of inductor is relative relaxed and could be up to 8 mm typically, so DCR (DC resistance) of today's discrete inductor in server motherboard design is usually within the range of 0.15 - 0.3 mohm by adopting thick copper of winding. Currently there are two most popularly adopted inductor skus, one is with DCR of 0.29 mohm, the other is with DCR of 0.19 mohm [7] [8]. For coupled inductor design for server application, it's also doable to design its DCR of each winding to same level, *i.e.*, DCR is controlled as 0.19mohm. So this paper will mainly focus on analysis of the impedance difference of the power trace and its impact from motherboard routing side, rather than on the DCRs of inductors themselves. Moreover, it's feasible to control the physical size (both land pattern and height) of one coupled inductor to be equivalent to the total size of two discrete inductors in a two phases buck VR design, so that we can keep aforementioned advantages of coupled inductor such as transient and efficiency improvements for VR without the sacrifice of increasing motherboard real estate.

2.1. Some Considerations for Coupled Inductor Layout Design

For coupled inductor design, as shown in **Figure 3**, there are two possible layouts in motherboard placement. **Figure 3(a)** is a lateral layout in which both first phase inductor L1 and second phase inductor L2 have extra PCB trace routing represented by Rd1 and Rd2 respectively. It's obvious Rd1 and Rd2 are closely identical so this is a balanced design. By contrast, **Figure 3(b)** is a vertical layout in which first phase inductor L1 has no extra PCB trace routing compared to that of a discrete inductor. Second phase inductor has more than 2 times extra PCB trace routing represented by Rc1 and Rc2 for back and forth routing. Obviously Rc1 is greater than Rd1 from straightforward comparison of trace routing length, and this is an imbalanced design.

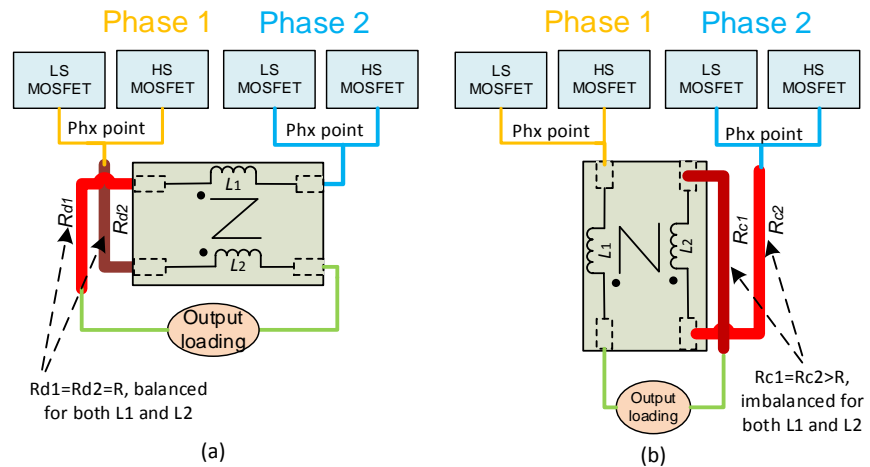


Figure 3. Two possible layouts for coupled inductor: (a). lateral layout (b). vertical layout.

Assuming $R_{d1} = R_{d2} = R$, then $R_{c1} = R_{c2} > R$. if each phase carries load current of I , it's easy to get total power loss from the extra PCB trace routing for both layouts:

$$P_{loss_lateral} = I^2 R_{d1} + I^2 R_{d2} = 2I^2 R \tag{1}$$

$$P_{loss_vertical} = I^2 (R_{c1} + R_{c2}) > 2I^2 R \tag{2}$$

It's derived that power loss from extra PCB trace routing for vertical layout is higher than that for lateral layout. Using the real coupled inductor (length = 17 mm, width = 10 mm) as an example the resistance of R_{c1} (R_{c2}) is roughly 1.7 times R_{d1} (R_{d2}), then total power loss from extra PCB trace routing for vertical layout is also roughly 70% higher than that for lateral layout. Besides, vertical layout of coupled inductor can cause potential current sharing and thermal imbalance between the two phases in spite of good current sharing scheme in today's VR controllers. In addition, the overall utilization of layout real estate for lateral layout is also better than vertical layout. Unless otherwise specified in this paper, all discussion and analysis are based on the lateral layout for coupled inductor in following sessions.

In the following, we will analyze several PCB layout schemes for coupled inductor design, then we will compare the difference of extra PCB trace routing for these schemes. Power DC CAD software, a well-known simulation tool for PCB layout in industry, is used to simulate resistance value of extra PCB trace routing for these schemes. Experimental test is also conducted to correlate to the simulation result of the first option (original design). It's to verify that Power DC is an accurate way to simulate DC resistance and so it's a reliable way to analyze other layout schemes without real implementations of those schemes.

2.2. Scheme 1—Original Layout

As shown in **Figure 4**, it's the original layout for coupled inductor power evaluation board. Two inductor winding symbols are also shown in the left snapshot (Top layer) to help easily understanding each winding routing direction and this

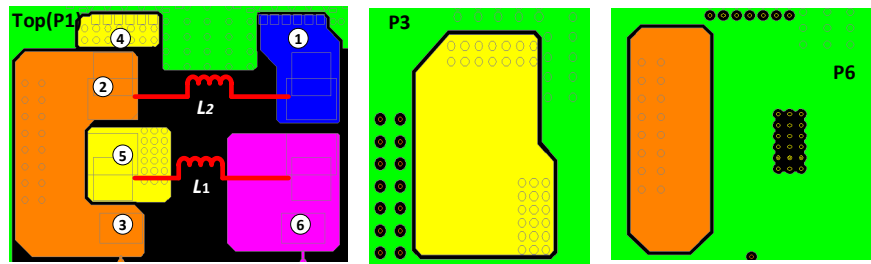


Figure 4. Original layout (Baseline) for coupled inductor power EVB.

is not shown anymore in after mentioned layout snapshots. This layout scheme has the following characteristics:

- Top layer is dominated and only limited utilization of internal layers (P3 and P6). the effectiveness of layer 6 (P6) is also limited. So resistance is bigger for extra PCB trace because vias location is relatively far from inductor pad to keep reasonable isolation space from power plane of P3.
- All internal GND layers are remained as complete ground layers.
- Impact on Internal layers is minimized, which is good for high speed signal routing and signal quality. Nevertheless, the overall occupancy of real estate on top layer is large, it could be a concern in real application.

2.3. Scheme 2—Adding More Layers for Layout

As shown in **Figure 5**, to improve the utilization of internal layers and reduce overall resistance of extra power trace routing, more internal layers (P3, P4, P6) and bottom layer (P8) are all used to route required traces for coupled inductor (L1, L2). This layout scheme is characteristic of the following:

- Top layer, bottom layer, more internal layers (P3, P4, P6) are utilized. So resistance could be reduced for extra PCB trace.
- All internal GND layers (P2, P5, P7) are kept complete.
- Impact on internal layers is minimized to benefit high speed signal routing and signal quality, and the overall occupancy of real estate on top layer is smaller and good for real application.

2.4. Scheme 3—Adding More Copper Pours for Top Layer

Figure 6 shows the other option of layout. It's similar to scheme 2 except for designing a complete copper pour on top layer. It's based on the fact that both outputs of L1 and L2 are tied together to the output of VR, so this small change can take full use of the available space on top layer to reduce the resistance of extra power trace routing.

2.5. Scheme 4—Adding More Vias for Layout

Figure 7 shows the last option by adding more vias into the routing area of extra power trace in scheme 3. The aforementioned three schemes actually have placed reasonable count of vias based on standard PCB routing guideline. This scheme is to investigate the impact of adding more vias. By the way, the inner

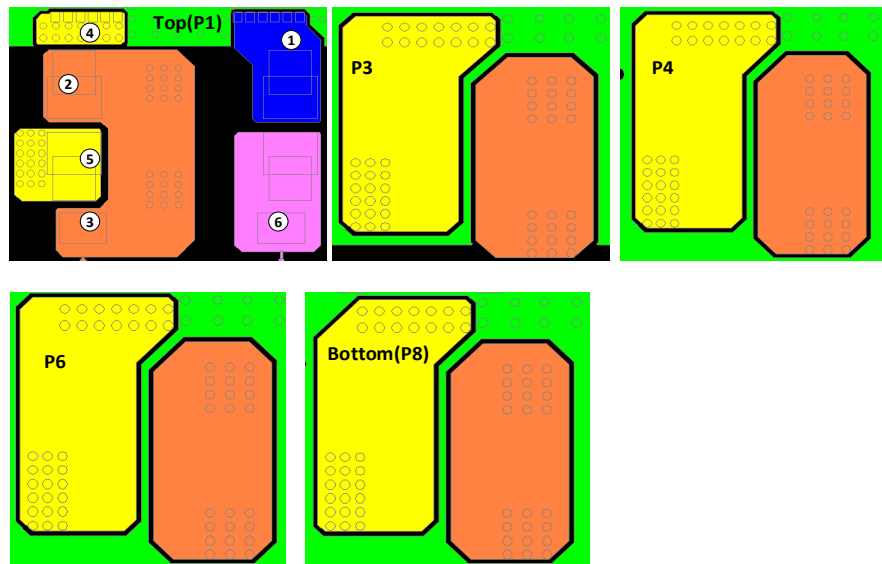


Figure 5. Scheme 2 improved layout by adding more internal layers.

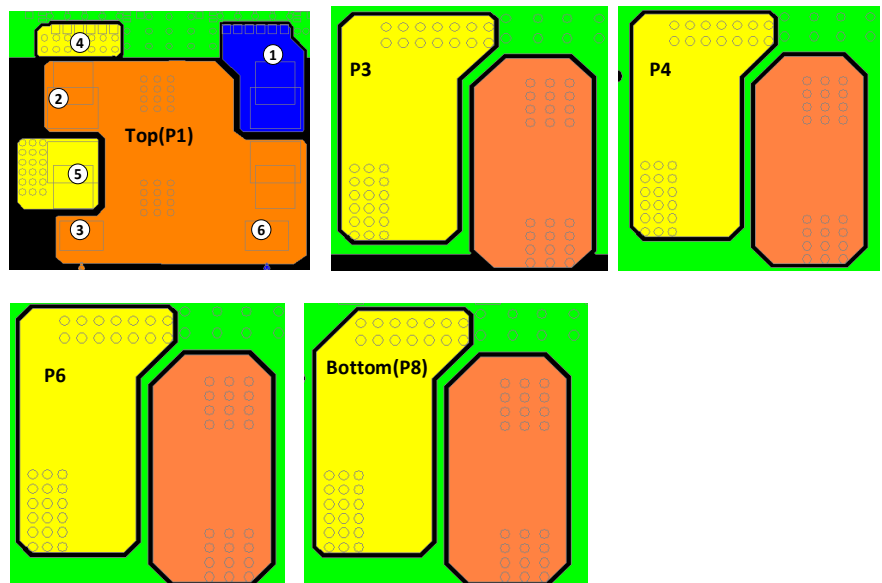


Figure 6. Scheme 3 improved layout by adding more copper pour on top layer.

diameter for all vias used in all layout schemes is 10mil and outer diameter is 20mil in size.

3. Simulation & Test Result

Power DC CAD software is used to simulate DC resistance of extra power trace routing under different layout schemes. The simulation results are shown in **Table 1**. As marked in **Figures 4-7**, the DC resistance from point 1 to point 3 (written as trace 1_3 in **Table 1**) represents extra power trace resistance of L2 and it could be split into two segments: point 1 to point 2 (written as trace 1_2 in **Table 1**) and point 2 to point 3 (written as trace 2_3 in **Table 1**). Similarly, the DC resistance from point 4 to point 6 (trace 4_6 in **Table 1**) represents extra

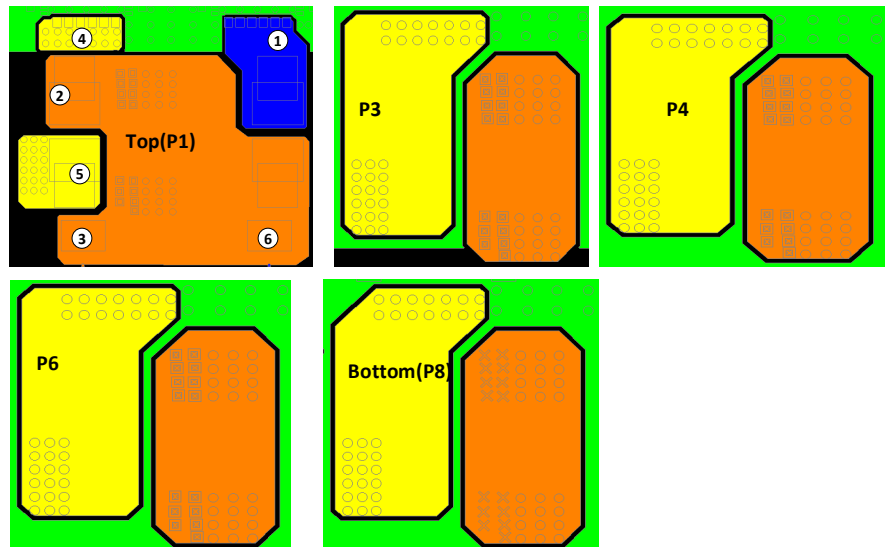


Figure 7. Scheme 4. improved layout by adding more vias.

Table 1. Impedance simulation result for coupled inductor in different layout options.

	scheme 1	scheme 2	scheme 3	Scheme 4
Trace*	(mohm)	(mohm)	(mohm)	(mohm)
4_6	1.353	0.94	0.889	0.874
4_5	0.913	0.506	0.501	0.501
5_6	0.44	0.434	0.388	0.373
1_3	1.61	1.602	0.966	0.945
1_2	0.54	0.602	0.586	0.586
2_3	1.07	1	0.38	0.359

*:exclude DCR, simulation assumed at 40 degree C.

power trace resistance of L1 and it could be separated into two segments: point 4 to point 5 (trace 4_5 in **Table 1**) and point 5 to point 6 (trace 5_6 in **Table 1**). Besides, one typical server core VR design with discrete inductor is selected to conduct simulation to obtain power path resistance of discrete inductor. The simulated data is shown in **Table 2** as comparison. Unless otherwise specified, all simulation data is based on two assumptions: a. at 40 degree C of copper temperature; b. exclusion of DCRs of both coupled and discrete inductors. So DCR is not a consideration in this paper.

It can be seen from **Table 1**:

- Original layout design (scheme 1) has the biggest extra power trace resistance with top layer routing dominated and limited internal layers utilized.
- By adding more internal layers, scheme 2 effectively reduces the associated resistance. Resistance of 4_6 for L1 is reduced around 30% (from 1.35 mohm to 0.94 mohm) and the reduction of resistance of 1_3 for L2 is very limited (from 1.61 mohm to 1.6 mohm). The ineffectiveness for the resistance reduction of 1_3 is mainly because those vias put at segment 2_3 are relatively far from the pad of inductor L2, thus the load current still mainly flows across

Table 2. Impedance simulation result for discrete inductor design.

Trace	Imp.(mohm)	Notes
1_6 (excl.DCR)	0.62	@40 degree C
DCR	0.19	

*DCR is from inductor spec, simulation based on 40 degree C.

top layer path and make those added internal layers less ineffective.

- Scheme 3 is mainly to optimize resistance of 1_3 by adding more copper pour at top layer. The reason is explained in scheme 2 description. It's effective because top layer copper plays a more important role. After this optimization, resistance of 4_6 and 1_3 is closed to each other and both are reduced by ~34% from the original design.
- In scheme 4, adding more vias to the segment of 2_3 helps further reduction of resistance of 1_3 and 4_6 but is very limited. This is because there has been enough vias in previous options and those vias are not as close as possible yet to the pad of inductor L2.

To have a fair comparison, one typical server core VR design (6 phases) with discrete inductor is selected to conduct simulation of power trace routing resistance for discrete inductor counterpart. As shown in **Figure 8**, the same length as that for coupled inductor is used for location point choice of layout from starting point to end point for the interested resistance. **Table 2** shows the simulation result for the PCB routing resistance for discrete inductor design. It can be seen that the extra PCB routing resistance for the original coupled inductor design is around 2.4X the discrete inductor design, and this number becomes around 1.4X after above mentioned layout optimization for the coupled inductor design. From the viewpoint of relative comparison, the difference is still big. However, from absolute resistance value standpoint, the equivalent resistance of PCB routing for coupled inductor design (after optimization) is only ~1/6 mohm in total so that its impact on overall efficiency is still limited in a 6 phases VR design. Some more quantitative data will be presented in the next section. Besides, DCR of the discrete inductor is only 0.19 mohm, around 30% of total inductor associated impedance. It indicates, from the viewpoint of inductor relevant copper loss reduction, the main focus is on PCB routing instead of inductor winding itself for future. It is also noted that only top layer is used for typical discrete inductor design in server motherboard with the perception that it will benefit EMC noise.

Table 3 shows simulated and measured resistance of power trace routing for original coupled inductor design. The accuracy is within around 10% range. It has been good enough from engineering standpoint if considering several factors: first, the copper thickness at top layer of real motherboard is typically more or less thicker than our theoretical data (1.5oZ), and it make simulation data little bit higher than what it should be; second, measuring such a sub-milliohm resistance is also a challenge, the test here is using one accurate DMM (digital multi-meter) to measure the voltage drop from switching point to the output

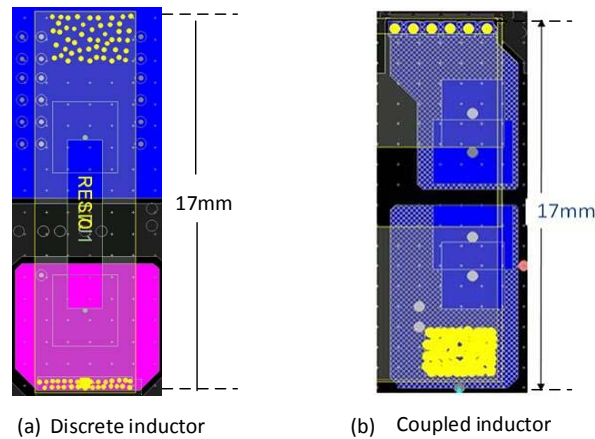


Figure 8. Simulation location for discrete inductor vs. coupled inductor.

Table 3. Measurement vs. simulation resistance in original coupled inductor EVB.

	Simulated	Measured	Error (%)
Trace*	(mom)	(mom)	
4_6	1.353	1.25	8.24%
1_3	1.61	1.45	11%

voltage point as marked in **Figure 4** by asserting a 10 A load current across the inductor. The temperature of copper of PCB top layer is also measured (40 degree C in this case) for simulation calibration.

4. Efficiency Impact & Overall Analysis

As shown in **Figure 9** and **Figure 10**, the efficiency curve for original coupled inductor design in a typical server CPU core VR is compared with that after considering removal of RMS loss of PCB routing extra trace resistance from coupled inductor. The aforementioned 8 layer power original EVB is used as baseline for comparison. It can be seen two efficiency curves overlaps almost within a whole load range from 0 A to 100 A. A more detailed efficiency delta is also plotted to illustrate more quantitative insights. It can be seen that the extra PCB routing trace resistance of coupled inductor causes about 0.8% efficiency suffering at full load current of 100 A if without any layout improvement, and this number becomes less than 0.3% after above mentioned layout improvement. At light load (less than 10 A), the efficiency suffering is less than 0.4% before layout improvement and the number is less than 0.15% after layout improvement. At CPU idle state (@6A load current), the efficiency suffering is around 0.2% before layout improvement and the number is less than 0.1% after layout improvement. There is some fluctuations for the curve of efficiency delta within load from 10 A to 100 A. It's mainly because there is phase count change from 2 phases to 6 phases with increase of load current and the overall loss distribution is not showing a monolithic trend. It can be concluded, after layout improvement, the overall efficiency impact from the extra PCB routing resistance is very

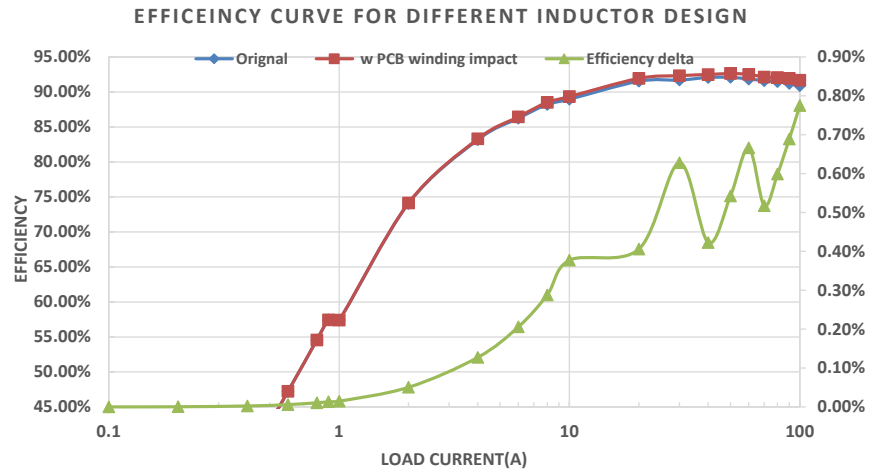


Figure 9. Efficiency impact analysis for original coupled inductor design before optimization.

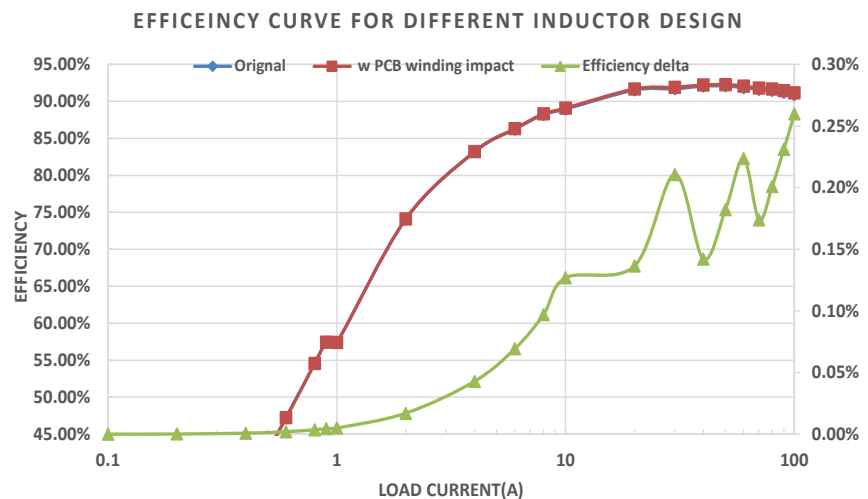


Figure 10. Efficiency impact analysis for coupled inductor design after optimization.

limited for the coupled inductor design.

Moreover, as can be seen from above analysis, discrete inductor design typically utilizes only top layer of motherboard as today's practice, while coupled inductor design has utilized more internal layers to optimize inductor routing resistance. Thus it's possible an argument that coupled inductor design could be noisier. It has the potential but it's a system level optimization task for EMC noise and beyond the scope of this paper. Nevertheless, there are some positive aspects to consider: First, the top layer copper usually could be thicker than standard stackup (1.5oz); Second, no high speed signals or sensitive signals are allowed to be routed under inductor area regardless of coupled or non-coupled inductor design, thus utilization of internal layers is not expected to cause obvious impact on signal quality or noise with careful layout design; Third, the statistics shows around 30% of servers in data center worldwide works at comatose

state [9]. It means efficiency at idle current also plays a very important role and above analysis shows the impact of extra PCB routing resistance on idle state efficiency is so minor to be ignored.

5. Conclusion

This paper quantitatively analyzes the impact of extra PCB routing impedance of coupled inductor design on the overall VR efficiency in a typical server system. It can be concluded that the efficiency impact after layout optimization is less than 0.3% at the worst case of full load current and the impact is minor to be ignored at light load. The coupled inductor design is still a promising solution given its overall benefits from other aspects.

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